Sequential Logic

- **Overview**
- **Set – Reset Flip-Flop**

(NOR Version) & (NAND Version)

General Form of Sequential Logic Design

Microprocessors & Computers

- Block diagram for PIC18(L)F2X/4XK22 series Low-Power, High-Performance Microcontrollers [1].

- Programme and data memory system
- Control system
- Arithmetic/maths/logic processing
- Digital I/O
- Analogue I/O
- Data buses
- Clock system
- Special functions and interfaces

- Used in embedded systems

[1] Datasheet DS41412D, 2010, Microchip Technology Inc.

Typical Storage Structure

Gated D-Type Flip-Flop

The Flip-Flop (NOR S-R)

Timing Diagrams

- Gates have Propagation Delay, T_{pd} .
- A Flip-Flop takes time to remember.
- Simple Timing Diagrams that count in T_{pd} can be used to explain their behaviour.

Timing Diagram for NOR S-R

- *Your graph here*

NAND S-R

Timing Diagram for NAND S-R

- *Your graph here*

Gated S-R Flip-Flop

Timing Diagram for Gated S-R

- *Your graph here*

Truth Table for Gated S-R

S	R	Q	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	-
1	1	1	-

S	R	Q+
0	0	Q
0	1	0
1	0	1
1	1	-

Excitation Table for Gated S-R

S	R	Q+
0	0	Q
0	1	0
1	0	1
1	1	-

=>

Q	Q+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

S-R Flip-Flop Circuit

S-R Flip-flop

Gated S-R latch.

For more details see http://en.wikipedia.org/wiki/Flip-flop_(electronics)

S-R Flip-Flop Symbol

Master Slave J-K Flip-Flop

J-K Flip-flop

J-K flip-flop Master Slave

Please read: http://en.wikipedia.org/wiki/Flip-flop_(electronics)#JK_flip-flop for more details

J-K Flip-Flop Symbol

Truth Table for J-K Action

J	K	Q	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

J	K	Q+
0	0	Q
0	1	0
1	0	1
1	1	nQ

Excitation Table for J-K Action

J	K	Q+
0	0	Q
0	1	0
1	0	1
1	1	Qn

=>

Q	Q+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

T Type Flip-Flop

T Flip-flop

For details please read:

http://en.wikipedia.org/wiki/Flip-flop_(electronics)

T Type Flip-Flop Symbol

Truth Table for T Action

T	Q	Q+
0	0	0
0	1	1
1	0	1
1	1	0

T	Q+
0	Q
1	nQ

Excitation Table for T Action

T	Q+
0	Q
1	nQ

=>

Q	Q+	T
0	0	0
0	1	1
1	0	1
1	1	0

D Type Flip-Flop

D Flip-flop

For details please read:

http://en.wikipedia.org/wiki/Flip-flop_(electronics)

D Type Flip-Flop Symbol

Truth Table for D Action

D	Q	Q+
0	0	0
0	1	0
1	0	1
1	1	1

D	Q+
0	0
1	1

Excitation Table for D Action

D	Q+
0	0
1	1

=>

Q	Q+	D
0	0	0
0	1	1
1	0	0
1	1	1

Gated J-K Flip-Flop

Gated J-K Flip-flop

Gated J-K latch.

For more details see http://en.wikipedia.org/wiki/Flip-flop_(electronics)

Timing Diagram for Gated J-K

- *Your graph here*

Buffered D Type

Timing Diagram for Buffered D

- *Your graph here*