Fundamentals of Electrical and Electronic Engineering

400462

Digital Electronics

Dr Ian M. Bell

Logic Building Blocks

We have already seen a number of logic circuits which are building blocks of larger systems.

Multiplexers
Seven Segment Decoder
Tristate bus buffers / transceivers
Adders
Subtractors

These functions can all be built using combinational logic (although more complex versions may also exist, particularly for arithmetic circuits)

They are typically combined with registers, which hold the data to be processed and the results of operations

There are other commonly used combinational functions, such as

1-of-N Decoders
Priority Encoders
Comparators
Parity Checkers

Digital designers are familiar with functions such as these33, and use then when appropriate without having to design them from scratch

Logic Building Blocks

- Many of the functions listed on the previous slide (and other similar functions) are available as individual (discrete) integrated circuits.
  - These ICs are used instead of building the circuits using basic gates
  - Even with this approach only small circuits can be built

- Logic design of larger circuits is “on-chip”, rather than using discrete ICs
  - Programmable logic devices (FPGAs etc.)
  - Custom ICs

- For on-chip design commonly used logic functions are also often available via the IC design software
  - These “virtual components” are called **IP blocks** (Intellectual Property)
  - Also called **IP Cores**

- Of course someone had to design the circuit block initially and if nothing is available to meet your need, you have to design that circuit.

Logic Building Blocks – IP Blocks

- IP blocks are available for basic functions but also for more complex and advanced functions which are commonly used in digital systems, e.g.
  - SDRAM controller
  - USB interface
  - Floating point multiplier

- As ICs are designed using software tools the IP blocks can be selected and configured by the design software
  - Unlike discrete ICs, which are fixed, IP blocks are synthesised when needed and can be flexible, offering options and variants
  - IP blocks typically designed using **Hardware Description Languages** (HDL) code, not schematics. Code may be hidden from users

- IP blocks may be purchased directly or provided with the design software when it is purchased
  - Open source IP blocks are also available

Example Discrete IC: Adder

IC manufacturer's web site provides technical overview and production status

https://www.onsemi.com/PowerSolutions/product.do?id=MC14008B

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MC14008B: 4-Bit Full Adder

Datasheet: 4-Bit Full Adder
Rev. 8 (103kB)

Product Overview

»View Reliability Data
»View Material Composition
» Product Change Notification

The MC14008B 4-bit full adder is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

Features

- Look-Ahead Carry Output
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-powerSchottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4008B
- Pb-Free Packages are Available*

Technical Documentation & Design Resources

Simulation Models (1) | Package Drawings (1)

Data Sheets (1)

Availability & Samples | Specifications | Case Outlines

Product	Status	Compliance	Description	Package		MSL*	Container		Budgetary Price/Unit
				Type	Case Outline		Type	Qty.	
MC14008BDR2G	Active	Pb-free Halide free	4-Bit Full Adder	SOIC-16	751B-05	1	Tape and Reel	2500	$0.2933 Sample Inventory

Example Discrete IC: Adder

Manufacturer's data sheet provides full technical data

MC14008B

4-Bit Full Adder

The MC14008B 4−bit full adder is constructed with MOS P−Channel and N−Channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look−ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high−speed operation when used with other adders in a system.

Features

- Look−Ahead Carry Output
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4008B
- This Device is Pb−Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

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SOIC−16
D SUFFIX
CASE 751B

PIN ASSIGNMENT

MARKING DIAGRAM

MC14008B

TRUTH TABLE
(One Stage)

C_{in}	B	A	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

BLOCK DIAGRAM

Example Discrete IC: Adder

This data related to timing – rise/fall times and LH/HL propagation delays

Note change of delays with capacitive load, as discussed in earlier lectures

MC14008B

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Sum in to Sum Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 127 ns		10	–	160	320	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	–	115	230	
Sum In to Carry Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 220 ns		5.0	–	305	610	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 112 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Carry In to Sum Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 290 ns		5.0	–	375	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 122 ns		10	–	155	310	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	–	115	230	
Carry In to Carry Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 85 ns		5.0	–	170	340	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 30 ns		15	–	55	110	

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

Example Discrete IC: Adder

ICs can be purchased from component suppliers / distributors

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Products | Manufacturers | Applications | Services & Tools | Help | Order History | Log In | Register | 0

All | Part No. / Keyword | In Stock | RoHS

All Products > Semiconductors > Logic ICs > Logic Adder & Subtractor > ON Semiconductor MC14008BDR2G

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Mouser No:	863-MC14008BDR2G
Mfr. No:	MC14008BDR2G
Mfr.:	ON Semiconductor
Customer No:	Customer No
Description:	Logic Adder & Subtractor LOG CMOS ARTH OP 4BIT
Datasheet:	MC14008BDR2G Datasheet
ECAD Model:	Build or Request PCB Footprint or Symbol

Download the free Library Loader to convert this file for your ECAD Tool.

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In Stock: 4,254

Stock:	4,254 Can Dispatch Immediately
On Order:	0
Factory Lead Time:	20 Weeks
Enter Quantity:	Minimum: 1 Multiples: 1 — Buy

Pricing (GBP)

Qty.	Unit Price	Ext. Price
Cut Tape / MouseReel™		
1	£0.45	£0.45
10	£0.369	£3.69
100	£0.225	£22.50
1,000	£0.174	£174.00

Using IP Blocks

- Access to IP blocks is typically via the design software for what ever system / platform / programmable device family you are working with
- Screenshot shows Intel Quartus FPGA design software
  - ❑ Left : IP catalog where available IP can be selected to add to the design
  - ❑ Right: an instance of the LPM_ADD_SUB IP block has been added to a schematic
  - ❑ Following slides slow configuration of and IP block

Using IP Blocks

As with discrete ICs IP blocks have datasheets / user guides

www.altera.com/literature/ug/ug_lpm_alt_mfug.pdf

Intel FPGA Integer Arithmetic IP Cores User Guide

Updated for Intel® Quartus® Prime Design Suite: **17.1**

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5 LPM_ADD_SUB (Adder/Subtractor)

The LPM_ADD_SUB IP core lets you implement an adder or a subtractor to add or subtract sets of data to produce an output containing the sum or difference of the input values.

The following figure shows the ports for the LPM_ADD_SUB IP core.

Figure 4. LPM_ADD_SUB Ports

5.1 Features

The LPM_ADD_SUB IP core offers the following features:

- Generates adder, subtractor, and dynamically configurable adder/subtractor functions.
- Supports data width of 1–256 bits.
- Supports data representation format such as signed and unsigned.
- Supports optional carry-in (borrow-out), asynchronous clear, and clock enable input ports.
- Supports optional carry-out (borrow-in) and overflow output ports.
- Assigns either one of the input data buses to a constant.
- Supports pipelining with configurable output latency.

Example FPGA IP Block: Adder/Subtractor

- Set number of bits
- Set mode: add, subtract or both
  - The add-subtract input is same idea as in the adder / subtractor discussed in an earlier lecture

Example FPGA IP Block: Adder/Subtractor

- Set input as both variable (normal add), or one fixed (add a constant)
- Set number type as signed or unsigned
  - Unsigned binary or two's compliment

Example FPGA IP Block: Adder/Subtractor

- Select which carry signals are used (carry in and out)
- Overflow is similar to carry, but specifically indicates result is outside numerical range of circuits output

Example FPGA IP Block: Adder/Subtractor

- Note block symbol changes to show addition I/O with options selected

Commonly used Logic Functions

The following slides will describe the following commonly used logic functions

1-of-N Decoders

Priority Encoders

Comparators

Parity Checkers

1-of-N Decoders

- The name *one-of-N decoder* describes what the outputs do
- It has ***N* outputs** and **one** of them is 'ON' (active) at a time
- *Active* output may be 1 or 0, the others are at the opposite level
- Which output is active is determined by a binary input number
- Example if input value is 5 (binary 101), output 5 will be 1 and others 0

Example circuit symbol

2-bit binary input

4 outputs

1-of-N Decoders

- Common sizes for these decoders include
  - 1-of-4 (2 bit binary in)
  - 1-of-8 (3 bit binary in)
  - 1-of-16 (4-bit binary in)
  - 1-of-10 (Binary Coded Decimal – BCD in)

- A BCD decoder can receive binary inputs greater than 9, in which case typical devices give an all-inactive output

- Commonly used to select one of several subcircuits to be active based on a binary address/selection signal

Active-High 1-of-4 Decoder

I_1	I_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Decoder IP Block

User selects number of bits and which outputs are available

Example use of 1-of-N Decoder

The decoder selects data from one of the four registers to pass onto the bus via the tristate drivers.

Which tristate is on is determined by the address value (when Enable is high)

If Enable is low all the tristate drivers will be off

Priority Encoder

- Like the opposite of a 1-of-N decoder. N inputs, binary number output
- Decides on the highest priority input which it is given, and produces a binary number which represents this
- May also have an output to indicate if any or no inputs are selected

Example: 4-Input Priority Encoder

I_0	I_1	I_2	I_3	Q_1	Q_0	V
0	0	0	0	0	0	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

I inputs
Q binary output
V "Valid" – a least one input active

8-input priority encoder

HEF4532B
MSI

DESCRIPTION

The HEF4532B is an 8-input priority encoder with eight active HIGH priority inputs (I_0 to I_7), three active HIGH outputs (O_0 to O_2), an active HIGH enable input (E_{in}), an active HIGH enable output (E_{out}) and an active HIGH group select output (GS).
Data is accepted on inputs I_0 to I_7. The binary code corresponding to the highest priority input (I_0 to I_7) which is HIGH, is generated on O_0 to O_2 if E_{in} is HIGH. Input I_7 is assigned the highest priority.
GS is HIGH when one or more priority inputs and E_{in} are HIGH. E_{out} is HIGH when I_0 to I_7 are LOW and E_{in} is HIGH. E_{in}, when LOW, forces all outputs (O_0 to O_2, GS, E_{out}) LOW.

Fig.1 Functional diagram.

TRUTH TABLE

INPUTS									OUTPUTS				
E_{in}	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	GS	O_2	O_1	O_0	E_{out}
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	L	L	H
H	H	X	X	X	X	X	X	X	H	H	H	H	L
H	L	H	X	X	X	X	X	X	H	H	H	L	L
H	L	L	H	X	X	X	X	X	H	H	L	H	L
H	L	L	L	H	X	X	X	X	H	H	L	L	L
H	L	L	L	L	H	X	X	X	H	L	H	H	L
H	L	L	L	L	L	H	X	X	H	L	H	L	L
H	L	L	L	L	L	L	H	X	H	L	L	H	L
H	L	L	L	L	L	L	L	H	H	L	L	L	L

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial

LOGIC EQUATIONS

$$O_2 = E_{in} \cdot (I_4 + I_5 + I_6 + I_7)$$
$$O_1 = E_{in} \cdot (I_2 \cdot \bar{I}_4 \cdot \bar{I}_5 + I_3 \cdot \bar{I}_4 \cdot \bar{I}_5 + I_6 + I_7)$$
$$O_0 = E_{in} \cdot (I_1 \cdot \bar{I}_2 \cdot \bar{I}_4 \cdot \bar{I}_6 + I_3 \cdot \bar{I}_4 \cdot \bar{I}_6 + I_5 \cdot \bar{I}_6 + I_7)$$
$$E_{out} = E_{in} \cdot \bar{I}_0 \cdot \bar{I}_1 \cdot \bar{I}_2 \cdot \bar{I}_3 \cdot \bar{I}_4 \cdot \bar{I}_5 \cdot \bar{I}_6 \cdot \bar{I}_7$$
$$GS = E_{in} \cdot (I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7)$$

Example use of Priority Encoder

Timers interrupt processor to carry out actions at specific time intervals

Alarm condition will override timer interrupts if they occur at the same time

Parity Encoders and Decoders

- Parity is a way to check if a digital data word has been corrupted
- Allows single bit errors (i.e. one bit in the wrong state) to be detected
- Works by adding an extra bit to the word we want to check
- Simple to implement in hardware
- Particularly useful where
    - Operation can be repeated if corruption is detected
    - Simply knowing an error occurred is useful

Comparators

A comparator compares two binary words

Identity comparator

Outputs a single bit to indicate if the two words are equal or not

If (A=B) then …

Magnitude comparator

Indicates if a binary number on one input is equal to, greater than, or less than a binary number on the other input

If (A=B) then …
If (A<B) then …
If (A>B) then …
If (A<=B) then …
If (A>=B) then …

Identity Comparator

E is an enable / expand input

Fig 2. Logic diagram

Fig 6. Example of cascading comparators

Comparator IP Block

User selects number of bits which outputs are required

Parity Encoders and Decoders

- Used to check for corruption in data transmission and data storage
- Specific uses include
  - RAM memory
  - PCI buses in computers
  - Microprocessor caches
  - Serial data transmission
  - Redundant Array of Independent Disks (RAID)

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Parity Encoders and Decoders

- Two types of parity
  - ***Even***: parity bit set so total number of high bits is an even number,
  - ***Odd***: parity bit set so total number of high bits is an odd number
- If one of the bits is subsequently corrupted (including the parity bit) the number of high bits will then be incorrect for the parity regime in use
- Example of even parity bit for several 8-bit words

01101001 0	4 1's (even, so 0 parity bit)
01110000 1	3 1's (odd, so parity bit is 1 so that total 1's is even)
01001000 0	2 1's (even, so 0 parity bit)
10111111 1	7 1's (odd, so parity bit is 1 so that total 1's is even)

Parity Check with no Data Error

Transmitter

Data to transmit	01101001	
Generate parity bit	01101001 ▶	0

Transmission OK	01101001	0

Receiver

Received data & parity	01101001	0
Generate parity from received data	01101001 ▶	0
Compare received and generated parity		
Data received OK	01101001	✓

Parity Check with Data Error

Transmitter

Data to transmit	01101001	
Generate parity bit	01101001 ▶	0

Corrupted transmission	01111001	0

Receiver

Received data & parity	01111001	0
Generate parity from received data	01111001 ▶	1
Compare received and generated parity		
Data Error Detected!	01111001	

Parity Encoder

- XOR gate provides an even parity bit for a 2 bit binary word
- To make larger parity generators use a tree of XOR gates

Parity Checker

logic diagram

Pin numbers shown are for the P, Q, and SO packages.