Fundamentals of Electrical and Electronic Engineering

400462

Digital Electronics

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Negative Numbers – Complements

Example using base 2, 2's Complement

-0110 in binary, 4 digit (bit) sign-magnitude numbers

Next power of two is 10000 (5 bits)

10000 – 0110 is 1010 *(16 – 6 = 10)*

1010 is the 4-bit 2's complement of -0110

- obtain the 2's complement we can
- **Invert all the bits and add 1** e.g. 0110➔1001➔1010
- This is easy to implement as a logic circuit

Subtraction Using Radix Complements

Example in base 10 (10's complement, 2 digits)

25 – 32

complement of 32 is 100 – 32 ➔ 68

so –32 is represented by 68

25 – 32

25 + (-32)

25 + 68 = 93

Result is 93

93 represents a negative number in 2-digit 10's complement

To convert to sign-magnitude: 100 – 93 ➔ 7

Result in sign-magnitude format is –7

Subtraction Using Radix Complements

Example in base 2 (2's complement, 4-bit numbers)

0011 – 0101 (3 – 5 in decimal)

2's complement of 0101 is 1010 + 1 ➔ 1011 (**invert bits, add 1**)

so –5 is represented by 1011

0011 – 0101

0011 + (-0101)

0011 + 1011 = 1110

Result is 1110

Note: result 1110 represents a negative number in 4-bit 2's complement

To convert to sign-magnitude 10000 – 1110 ➔ 0010

or invert and add one: 1110 is 0001 + 1 ➔ 0010 (**invert bits, add 1**)

Negative number, so binary sign-magnitude version is written -0010

Result is –2 in decimal sign-magnitude format

Negating numbers and Subtraction

To make a number negative we “invert all bits” and “add 1”

If we have an adder S=A+B we can do a subtraction if we make B negative

Then we have S=A-B

So the adder could do both addition and subtraction

We need a circuit to either “invert all bits” or not as required

XOR gates can be used for this purpose

The carry-in of the adder can be used to “add one”

XOR is a “Controlled Inverter”

Control	Data	Out
0	0	0
0	1	1
1	0	1
1	1	0

Non inverting

Inverting

Adder/Subtractor

This is an adder/subtractor circuit based on the preceding discussion

Block Diagram: Adder/Subtractor with input/output resisters

Register storing results of Y+X or Y-X

Registers storing input values X and Y and add/subtract control

Registers store data and results

This is a typical digital circuit structure in which data to be processed is stored in a set registers and results are stored in another register

Block Diagram: Adder/Subtractor with input/output registers

This is circuit performs the operations

RESULT = X0 + Y0 if ADDSUB = 0

RESULT = X0 - Y0 if ADDSUB = 1

X0 and Y0 are 8 bits, RESULT is 9 bits

Signals

X0 Data input

Y0 Data input

ADDSUB Add/Subtract control input

X1 Register stored version of X0

Y1 Register stored version of Y0

ADDSUB1 Registered ADDSUB

PMX1 Plus or Minus X1

ASXY Add/subtract X and Y

CARRY Carry from X,Y add/subtract

RESULT registered result of operation

CLOCK clock for all registers (not shown)

Some notes about drawing block diagrams

A block diagram shows the interconnection of larger subcircuits, rather than showing individual gates and flipflops

Some notes about drawing block diagrams

Some notes about drawing block diagrams

Signals such as clocks and reset may be omitted if there is no ambiguity about their wiring

Data Routing within Systems

So far we have looked at examples of circuits which can

- Perform logical and decision making operations (Boolean algebra etc.)
- Code/decode between data formats (e.g. seven segment decoder)
- Store data to be processed or store the results (flipflops/registers)
- Perform mathematical operations on numerical data (adders etc.)

Another key aspect of digital circuits and systems is getting data from one part of a system to another. For example

- From a microprocessor to/from a set of memory devices
- Selecting which data to send to arithmetic circuit for processing

Key approaches to data movement, selection and routing are

- **Multiplexers** – multiple inputs, one way to a single destination
- **Buses** – multiple sources and destinations, both directions

Multiplexers (MUX)

- Used for data routing
- Select one of a set of possible inputs and convey data on that input to the output
- Can be thought of as electronic mutli-way switch
- Important building block in digital systems
- The select inputs are usually binary coded

  Mux with 4 data inputs (like a 4 position switch) will have two select inputs on which the binary numbers (00, 01, 10, 11) result in a different input being routed to the output
- Can handle multi-bit data (e.g. four 8-bit inputs switched to one 8-bit output)

Multiplexers

This is the simplest multiplexer – a one bit two way multiplexer

It is like single pole two way switch

Symbol

Functional concept

4-Bit 2-Way Multiplexer Symbol – Showing All I/O Bits

4-Bit 2-Way Multiplexer Symbol – I/O Shown as Buses

Multiplexers

This is the simplest multiplexer – a one bit two way multiplexer

It is like single pole two way switch

Symbol

Functional concept

Functional table

S	Q
0	I_0
1	I_1

Full truth table

S	I_0	I_1	Q
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Multiplexers

- The multiplexer can be implemented using logic gates

S	I_0	I_1	Q
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

- An alternative possibility is to use MOS switches more directly

MOS Transistor as a Switch - Again

- We have seen the MOSFET used a switch in logic gates
  - Here it connects the output to either the supply or ground to give a logic 1 or logic 0
- **The MOS switch can also be use to**
  - Route signals through a circuit
  - Isolate the output of a circuit so that other circuits can take control of the signal

Equivalent circuit

Transistor circuit

Capacitor charging via an NMOS switch

We need to understand how the MOS transistor behaves when we try to use it to route signals

- Consider a logic 1 being switched through an NMOS transistor (V_T = 1V)

- Output reaches input logic 1 voltage minus threshold voltage
- At this point the transistor turns off – so voltage does not increase further
- **NMOS signal routing switch degrades logic 1 voltage level**
- A gate must be used to restore good logic level

A similar argument shows that PMOS transistor routing switches degrade the logic 0 voltage

CMOS Signal Routing Switches

- MOS transistors can be used as logic signal routing switches, **but**
  - NMOS transistors degrade the logic 1 voltage
  - PMOS transistors degrade the logic 0 voltage

- A gate can be used to restore good logic levels, **but**
  - One routing switch must not be used to directly control another

- If we use an NMOS and a PMOS transistor in parallel for signal routing logic levels are not degraded
  - This is known as a CMOS transmission gate

CMOS Transmission Gate

Switch equivalent

Basic schematic

Detailed schematic

Symbol

Multiplexers

- An alternative possibility is to use MOS switches more directly

- We need two MOS switches controlled by opposite logic levels from S

Multiplexers

- One-bit two-way multiplexer implemented using CMOS transmission gates

Multiplexer Implementations

- The multiplexer can be implemented two very different ways
- This sort of situation is not unusual in digital electronics
- Often when designing larger systems the internal structure of building blocks such as multiplexers may not be known to the designer

Buses

Interconnection of subsystems

Point to point communication

Shared bus-based communication

- Shared buses allow many subsystems to communicate without excessive quantities and complexity of wiring. Commonly used in computer systems.
- Any two devices on the bus can communicate at one time
- Usually one device (e.g. a microprocessor) is in control of the bus (bus master) and selects which other device (slave) it will communicate with
- If there are multiple masters some form of decision-making process (arbitration) is required to determine which master accesses the bus

Tristate Buses

- As multiple logic outputs may put signals onto the same interconnection (wires), the system must be designed to prevent clashes
- Commonly **tristate buffers** are used to put (***write***) signals onto a bus
- Buffers used to put signals onto buses are called **bus drivers**
- One buffer on a buss wire can be active at any one time, all others are high impedance, which their outputs disconnected from the bus
- When one signal is on the bus other subsystems can read input (***read***) the value from the bus.

Tristate Outputs

Tristate outputs can be disconnected from the rest of the circuit (put into a high impedance state, Z)

Tristate Inverter

Concept

Truth table

E	I	Q
0	0	Z
0	1	Z
1	0	1
1	1	0

Symbol

The Enable input, E, determines if the gate outputs follow its normal logic function or are disconnected

Tristate Outputs

Tristate Buffer

Concept

Truth table

E	I	Q
0	0	Z
0	1	Z
1	0	0
1	1	1

Symbol

Example implementation of tristate inverter

Timing Diagram of Tristate Inverter

Tristate Connections onto a Bus

Drawing the Bus as a Multi-bit Single Line

Drawing the Bus and data Sources as Single Multi-bit Lines

Transfer Data from P onto Bus

Transfer Data from Q onto Bus

Bus Contention

Bus Timing Diagram Example

There are times delays from

- The bus driver enable signal going on to the data appearing on the bus (**e**nable).

  $\mathbf{t_{eQ}}$ and $\mathbf{t_{eP}}$

- The bus driver enable going off to the bus returning to high impedance (**d**isable).

  $\mathbf{t_{dQ}}$ and $\mathbf{t_{dP}}$

What happens next?

Complete the timing diagram for the bus in response to the control signals E_P and E_Q

Bidirectional Bus Buffer / Bus Transceiver

A bidirectional bus buffer allows data to be transferred in either direction between two buses (A and B), or for the two buses to be isolated from one another

Bus transceivers may be level-shifting to allow data flow between buses operating at different voltages

SN74ALVC164245 16-Bit 2.5-V to 3.3-V or 3.3-V to 5-V Level-Shifting Transceiver With 3-State Outputs

1 Features

- Member of the Texas Instruments Widebus™ Family
- Maximum t_{pd} of 5.8 ns at 3.3 V
- ±24-mA Output Drive at 3.3 V
- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Applications

- Electronic Points of Sale
- Printers and Other Peripherals
- Motor Drives
- Wireless and Telecom Infrastructures
- Wearable Health and Fitness Devices

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74ALVC164245	TSSOP (48)	12.50 mm × 6.10 mm
	SSOP (48)	15.88 mm × 7.49 mm
	BGA MICROSTAR JUNIOR (56)	7.00 mm × 4.50 mm
	BGA MICROSTAR JUNIOR (54)	8.00 mm × 5.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

3 Description

This 16-bit (dual-octal) noninverting bus transceiver contains two separate supply rails. B port has V_{CCB}, which is set to operate at 3.3 V and 5 V. A port has V_{CCA}, which is set to operate at 2.5 V and 3.3 V. This allows for translation from a 2.5-V to a 3.3-V environment, and vice versa, or from a 3.3-V to a 5-V environment, and vice versa.

The SN74ALVC164245 is designed for asynchronous communication between data buses. The control circuitry (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) is powered by V_{CCA}.

To ensure the high-impedance state during power up or power down, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

Pin Configuration

DGG and DL Packages
48-Pin TSSOP and BGA MICROSTAR JUINIOR
Top View

Logic Diagram (Positive Logic)

Bidirectional Bus Buffer / Bus Transceiver

A bidirectional bus buffer allows data to be transferred in either direction between two buses (A and B), or for the two buses to be isolated from one another

$\overline{\text{Enable Output}}$	Direction Control	Action of Circuit
0	0	Data transferred: B ➔ A
0	1	Data transferred: A ➔ B
1	0	Both buses trisate, no transfer
1	1	Both buses trisate, no transfer

Bidirectional Bus Buffer

Bidirectional Bus Buffer – Transfer B to A

Bidirectional Bus Buffer – Transfer A to B

Bidirectional Bus Buffer – Isolate A and B